

a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels, and each of the plurality of addresses including a least significant data bit and a plurality of non-least significant data bits; and

a repair router to utilize the least significant data bit of at least one of the plurality of addresses to hold non-least significant information[.] from any of the plurality of non-least significant data bits.

20. (Amended) An integrated circuit comprising:

a memory device having an input data bus and an output data bus; and
first and second repair routers coupled to the input data bus and the output data bus, respectively, the first and second repair routers including routing circuitry to route data to and from the memory device as a function of defects in the memory device[.];

wherein the first and second repair routers include internal routing circuitry to utilize any non-least significant bit of the memory device as a least significant bit.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 3, 2002, and the references cited therewith.

Claims 7, 8, 15, and 20 have been amended, and no claims have been canceled or added; as a result, claims 1-23 are now pending in this application.

Rejections Under 35 U.S.C. §102

Claims 1-2, 9-10, 14, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by Ferris (U.S. Patent No. 5,163,023). Applicant respectfully traverses this rejection.

The Office Action alleges that routing circuitry 8 of Ferris teaches the following limitation as recited in claim 1: “repair router having internal routing circuitry to route *any* of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus.” Applicant respectfully disagrees.

The Examiner's attention is directed to Figure 3 of Ferris, where routing circuitry for the Nth group of columns BIT N is shown in some detail as logic circuits 80_N and 82_N. As can be seen in Figure 3, and as described at col. 5, lines 35-40, logic circuits 80_N and 82_N can "enable the column of the Nth group ... to be connected to the Nth bit position in the data bus via a 'straight' path or, during redundancy, enable the column of the N=1th group ... to be connected to the Nth position in the data bus via a 'shift' path." Figure 4 of Ferris also shows routing circuitry 8 with "straight" and "shift" paths. Figure 4 of Ferris clearly shows that only the bit position adjacent to the least significant bit can be connected to the least significant bit (see ST₀, SH₀, and ST₁ of Figure 4). Accordingly, applicant respectfully submits that Ferris's routing circuitry 8 only teaches connecting a bit position to an adjacent bit position, and does not teach the ability to route any of the non-least significant bits to the least significant bit as claimed in claim 1.

With respect to claim 2, applicant respectfully submits that Ferris does not disclose, teach, or suggest repair routing circuitry to route any of the non-least significant bits to the next-to-least significant bit as alleged in the office action. As discussed above, Ferris only discloses a "straight" path and a "shift" path for each bit, and does not teach the routing of any non-least significant bit to the next-to-least significant bit.

With respect to independent claim 9, the office action applies the same reasoning as given for claim 1. Applicant respectfully submits that Ferris does not disclose, teach, or suggest the subject matter of claim 9, including for example, "the first repair router including routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the least significant bit of at least one of the plurality of addressable memory locations." [Emphasis added]. Claim 10 depends on claim 9 and is believed to be in condition for allowance at least by virtue of dependency.

With respect to claim 14, applicant respectfully submits that Ferris does not disclose, teach, or suggest repair routing circuitry to route any of the non-least significant bits to the next-to-least significant bit as alleged in the office action. As discussed above, Ferris only discloses a "straight" path and a "shift" path for each bit, and does not teach the routing of any non-least significant bit to the next-to-least significant bit.

With respect to claim 20, the office action alleged that “the claim has substantially the limitations of claim 1.” Applicant respectfully disagrees. Further, claim 20 has been amended to include “wherein the first and second repair routers include internal routing circuitry to utilize any non-least significant bit of the memory device as a least significant bit.” Applicants respectfully submit that claim 20 defines over the references of record.

Accordingly, applicant respectfully submits that the rejection of claims 1-2, 9-10, 14, and 20 under 35 U.S.C. §102(b) has been overcome, and the claims are in condition for allowance.

Rejections Under 35 U.S.C. §103

Claims 3-8 and 11-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ferris in view of Shieltz (U.S. Patent No. 4,456,957). Applicant respectfully traverses this rejection on the basis that a proper *prima facie* showing of obviousness has not been established. Applicant submits that a proper *prima facie case* of obviousness has not been established in part because the combination of Ferris and Shieltz does not disclose, teach, or suggest the subject matter of claims 3-8 and 11-13.

Shieltz describes a router module to enable several data entry terminals to utilize a printer module. See the abstract of Shieltz. Figure 4 of Shieltz is cited in the office action in support of the rejection. Figure 4 of Shieltz shows router modules connected between “cassette terminals,” “terminals,” and “printer modules.” The router modules shown in Figure 4 of Shieltz are shown in more detail in Figure 1, which is described at col. 1, line 61 to col. 3, line 16 and beyond, as a router that routes data between cassettes, terminals, and printers. For example, at col. 3, lines 16, Shieltz states that “an important feature of this invention is that the router module 20 (Fig. 1) enables the terminals like 24 and 26, for example, to communicate with each other without the intervention of a complex computer system as earlier explained herein.” Applicant respectfully submits that Shieltz does not describe a “repair router” or anything that routes bits from one significance to another, nor does Shieltz describe multiple repair routers on either side of a memory device.

With respect to claim 3, applicant respectfully submits that neither Ferris nor Shieltz, taken alone or in combination, disclose, teach, or suggest the subject matter of claim 3, including

for example, “a second repair router having a second repair router input data bus coupled to the memory device output data bus.”

Further with respect to claims 6-8, applicant respectfully submits that neither Ferris nor Shieltz taken alone or in combination, disclose, teach, or suggest a “display device.” Claims 7 and 8 have been amended to provide proper antecedent basis without a change in scope. These amendments have not been made for reasons of patentability.

With respect to claim 11, applicant respectfully submits that neither Ferris nor Shieltz, taken alone or in combination, disclose, teach, or suggest the subject matter of claim 11, including for example, “the second repair router including routing circuitry to reverse any routing performed by the first repair router.”

With respect to claim 12, applicant respectfully submits that neither Ferris nor Shieltz, taken alone or in combination, disclose, teach, or suggest the subject matter of claim 12, including for example, “wherein the first repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations.”

With respect to claim 13, applicant respectfully submits that neither Ferris nor Shieltz, taken alone or in combination, disclose, teach, or suggest the subject matter of claim 13, including for example, “the second repair router including routing circuitry to reverse any routing performed by the first repair router.”

Accordingly, applicant respectfully submits that the rejection of claims 3-8 and 11-13 under 35 U.S.C. §103(a) has been overcome, and the claims are in condition for allowance.

Claims 15-19 and 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ferris in view of Lindsay (U.S. Patent No. 6,330,693).

Claim 15 has been amended. Applicants respectfully submit that neither Ferris nor Lindsay, taken alone or in combination, disclose, teach, or suggest the subject matter of claims 15-19, including for example, “a repair router to utilize the least significant data bit of at least

one of the plurality of addresses to hold non-least significant information from any of the plurality of non-least significant data bits.”

Claims 21-23 depend from claim 20, which, as discussed above, is believed to be in conditions for allowance, and applicant respectfully submits that claims 21-23 are also in condition for allowance at least by virtue of dependency.

Accordingly, applicant respectfully submits that the rejection of claims 15-19 and 21-23 under 35 U.S.C. § 103(a) has been overcome, and the claims are in condition for allowance.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2159 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 16 day of September, 2002.

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Signature



Clean Version of Pending Claims

REPAIRABLE MEMORY IN DISPLAY DEVICES

Applicant: Samson X. Huang

Serial No.: 09/675,067

1. An apparatus comprising:
 - a memory device having a memory device input data bus including a least significant bit and a plurality of non-least significant bits; and
 - a first repair router having a first repair router input data bus including a least significant bit and a plurality of non-least significant bits, and a first repair router output data bus coupled to the memory device input data bus, the first repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus.
2. The apparatus of claim 1 wherein:
 - the plurality of non-least significant bits includes a next-to-least significant bit; and
 - the first repair router further includes additional repair routing circuitry to route any of the non-least significant bits to the next-to-least significant bit.
3. The apparatus of claim 1 wherein the memory device includes a memory device output data bus including a least significant bit and a plurality of non-least significant bits, the apparatus further comprising:
 - a second repair router having a second repair router input data bus coupled to the memory device output data bus, and having a second repair router output data bus including a least significant bit and a plurality of non-least significant bits, the second repair router having internal routing circuitry to route the least significant bit of the memory device output data bus to any of the plurality of non-least significant bits of the second repair router output data bus.

4. The apparatus of claim 3 wherein the memory device includes a plurality of address ranges, and the first and second repair routers include address decoding circuitry to decode each of the plurality of address ranges.

5. The apparatus of claim 4 wherein the memory device includes two address ranges defined by a state of a most significant address bit.

6. The apparatus of claim 3 further comprising a display device coupled to the second repair router output data bus.

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7. (Amended) The apparatus of claim 6 wherein the display device is a color display device, and the memory device and first and second repair routers influence a first color of the color display device, the apparatus further comprising:

a1
a second memory device; and

a second pair of repair routers coupled to the second memory device to influence a second color of the color display device.

8. (Amended) The apparatus of claim 7 further comprising:

a third memory device; and

a third pair of repair routers coupled to the third memory device to influence a third color of the color display device.

9. A memory device comprising:

a plurality of addressable memory locations, each including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a repair router input data bus with a least significant bit and a plurality of non-least significant bits, and having a repair router output data bus coupled to the

plurality of addressable memory locations, the first repair router including routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the least significant bit of at least one of the plurality of addressable memory locations.

10. The memory device of claim 9 wherein:

the plurality of addressable memory locations are arranged into a plurality of address ranges; and

the first repair router further includes address decoding circuitry to decode each of the plurality of address ranges.

11. The memory device of claim 10 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

12. The memory device of claim 9 wherein the first repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations.

13. The memory device of claim 9 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

14. The memory device of claim 9 wherein:

the plurality of non-least significant bits includes a next-to-least significant bit; and

the first repair router further includes routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the next-to-least significant bit of at least one of the plurality of addressable memory locations.

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15. (Amended) A display system comprising:
a display device having an array of pixels;
a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels, and each of the plurality of addresses including a least significant data bit and a plurality of non-least significant data bits; and
a repair router to utilize the least significant data bit of at least one of the plurality of addresses to hold non-least significant information from any of the plurality of non-least significant data bits.

16. The display system of claim 15 wherein the display device is a silicon light modulator.

17. The display system of claim 15 wherein the memory is configured to hold a first color information, the display system further comprising:

a second memory configured to hold second color information; and
a second repair router coupled to the second memory.

18. The display system of claim 17 further comprising:

a third memory configured to hold third color information; and
a third repair router coupled to the third memory.

19. The display system of claim 15 wherein:

the plurality of addresses are arranged in a plurality of groups; and

the repair router includes routing circuitry to utilize the least significant bits of each of the plurality of groups separately.

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20. (Amended) An integrated circuit comprising:

a memory device having an input data bus and an output data bus; and
first and second repair routers coupled to the input data bus and the output data bus,
respectively, the first and second repair routers including routing circuitry to route data to and
from the memory device as a function of defects in the memory device;

wherein the first and second repair routers include internal routing circuitry to utilize any
non-least significant bit of the memory device as a least significant bit.

21. The integrated circuit of claim 20 further comprising a reflective electrode coupled to the memory, the reflective electrode having a plurality of pixels responsive to data from the memory device as received by the second repair router.

22. The integrated circuit of claim 21 wherein:
the memory device includes a plurality of groups of data locations; and
the first and second repair routers each include circuitry to separately route data for each of the plurality of groups of data locations.

23. The integrated circuit of claim 22 further comprising:
second and third memory devices; and
second and third pairs of repair routers coupled to the second and third memory devices respectively.